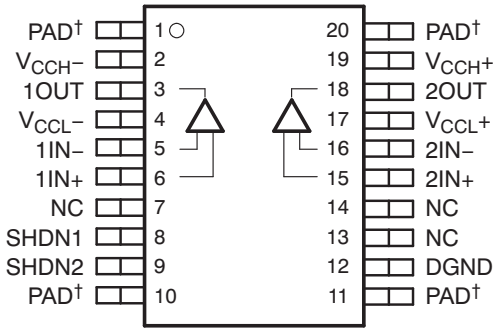
LOW-POWER ADSL CENTRAL-OFFICE LINE DRIVER

Check for Samples: THS6032

FEATURES

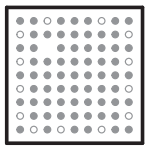
- **Low-Power ADSL Line Driver Ideal for Central Office**
  - **1.35-W Total Power Dissipation for Full-Rate ADSL Into a 25-Ω Load**
- **Low-Impedance Shutdown Mode**
  - **Allows Reception of Incoming Signal During Standby**
- **Two Modes of Operation**
  - **Class-G Mode: 4 Power Supplies, 1.35 W Power Dissipation**
  - **Class-AB Mode: 2 Power Supplies, 2 W Power Dissipation**
- **Low Distortion**
  - **THD = –62 dBc at f = 1 MHz, $V_{O(PP)}$ = 20 V, 25-Ω Load**
  - **THD = –69 dBc at f = 1 MHz, $V_{O(PP)}$ = 2 V, 25-Ω Load**
- **400-mA Minimum Output Current Into a 25-Ω Load**
- **High-Speed:**
  - **65-MHz Bandwidth (–3dB) , 25-Ω Load**
  - **100-MHz Bandwidth (–3dB) , 100-Ω Load**
  - **1200-V/µs Slew Rate**
- **Thermal Shutdown and Short-Circuit Protection**
- **Evaluation Module Available**

THERMALLY-ENHANCED SOIC (DWP)
PowerPAD™ PACKAGE
(TOP VIEW)

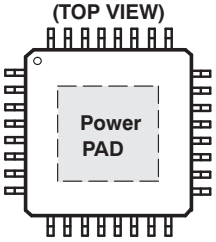


NC – Not Connected
† This terminal is internally connected to the thermal pad.

MicroStar Junior™ (GQE) PACKAGE
(TOP VIEW)



VFP PACKAGE
(TOP VIEW)



HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	5 V	±5 V	±15 V	DESCRIPTION
THS6002	•	•		•	•	500-mA differential line driver and receiver
THS6012	•			•	•	500-mA differential line driver
THS6022	•			•	•	250-mA differential line driver
THS6032	•			•	•	500-mA low-power ADSL central-office line driver
THS6062		•	•	•	•	Low-noise ADSL receiver
THS6072		•		•	•	Low-power ADSL receiver
THS7002		•		•	•	Low-noise programmable-gain ADSL receiver

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The THS6032 is a low-power line driver ideal for asymmetrical digital subscriber line (ADSL) applications. This device contains two high-current, high-speed current-feedback drivers, which can be configured differentially for driving ADSL signals at the central office. The THS6032 features a unique class-G architecture to lower power consumption to 1.35 W. The THS6032 can also be operated in a traditional class-AB mode to reduce the number of power supplies to two.

The class-G architecture supplies current to the load from four supplies. For low output voltages (typically $–2.5 < V_O < +2.5$), some of the output current is supplied from the $+V_{CC(L)}$ and $–V_{CC(L)}$ supplies (typically ±5 V). For large output voltages (typically $V_O < –2.5$ and $V_O > +2.5$), the output current is supplied from $+V_{CC(H)}$ and $–V_{CC(H)}$ (typically ±15 V). This current sharing between $V_{CC(L)}$ and $V_{CC(H)}$ minimizes power dissipation within the THS6032 output stages for high crest factor ADSL signals.

The THS6032 features a low-impedance shutdown mode, which allows the central office to receive incoming calls even after the device has been shut down. The THS6032 is available packaged in the patented PowerPAD ™ package. This package provides outstanding thermal characteristics in a small-footprint surface-mount package, which is fully compatible with automated surface-mount assembly procedures. It is also available in the new MicroStar Junior ™ BGA package. This package is only 25 mm^2 in area, allowing for high-density PCB designs.

Shutdown (SHDN1 and SHDN2) allows for powering down the internal circuitry for power conservation or for multiplexing. Separate shutdown controls are available for each channel on the THS6032. The control levels are TTL compatible. When turned off, each driver output is placed in a low impedance state which is determined by the voltage at DGND. This virtual ground at the outputs allows proper termination of a transmission line.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES			
	PowerPAD PLASTIC SMALL OUTLINE (2) (DWP)	PowerPAD PLASTIC MSOP (3) (GQE)	PowerPAD TQFP (VFP)	EVALUATION MODULES
0°C to +70°C	THS6032CDWP	THS6032CGQER	THS6032CVFP	THS6032 EVM (DWP package) THS6032GQE EVM (GQE package)
–40°C to +85°C	THS6032IDWP	THS6032IGQER	THS6032IVFP	—

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The DWP packages are available taped and reeled. Add an R suffix to the device type (for example, THS6032CDWPR).
(3) The GQE packages are only available taped and reeled.

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ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			VALUE	UNIT
$V_{CC(L)}$ and $V_{CC(H)}$	Supply voltage(2)		33	V
V_I	Input voltage		$\pm V_{CCH}$	
I_O	Output current(3)		800	mA
V_{ID}	Differential input voltage		±4	V
	Total power dissipation at (or below) 25°C free-air temperature(3)		See Dissipation Ratings Table	
T_J	Maximum junction temperature		+150	°C
T_A	Operating free-air temperature	C-suffix	0 to +70	°C
		I-suffix	–40 to +85	°C
T_{stg}	Storage temperature		–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $V_{CC(L)}$ must always be less than or equal to $V_{CC(H)}$.
(3) The THS6032 incorporates a PowerPAD on the underside of the chip. This acts as a heat sink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See the *Thermal Information* section for more information about using the PowerPAD thermally-enhanced packages.

DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = +25°C POWER RATING
DWP	21.5	0.37	5.8 W
GQE	37.8	4.56	3.3 W
VFP	30	1.2	4.1 W

(1) This data was taken using 2 oz. trace and copper pad that is soldered directly to a JEDEC standard 4 layer 3 in × 3 in PCB.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC(L)}$ – Class G mode	±3	±5	$\pm V_{CCH}$	V
		$V_{CC(L)}$ – Class AB mode	0	0	0	
		$V_{CC(H)}$	±5	±15	±16	
T_A	Operating free-air temperature	C-suffix	0		+70	°C
		I-suffix	–40		+85	

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ELECTRICAL CHARACTERISTICS

At $V_{CC(L)}$ = ±5 V, $V_{CC(H)}$ = ±15 V, R_L = 25 Ω, and T_A = +25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		THS6032 MIN	THS6032 TYP	THS6032 MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small signal bandwidth (–3 dB)	Gain = 1, R_F = 1.3 kΩ	R_L = 25 Ω		65		MHz
			R_L = 100 Ω		100		
		Gain = 2, R_F = 1.1 kΩ	R_L = 25 Ω		60		MHz
			R_L = 100 Ω		70		
	Bandwidth for 0.1-dB flatness	Gain = 1			30		MHz
		Gain = 2			25		
	Full-power bandwidth(1)	V_{OPP} = 20 V			19		MHz
SR	Slew rate(2)	Gain = 5, $V_{O(PP)}$ = 20 V			1200		V/µs
t_s	Settling time to 0.1%	Gain = 1, R_L = 25 Ω, 5-V Step			120		ns
NOISE/DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V_O = 20 V(pp), Gain = 5, f = 1 MHz			–62		dBc
		V_O = 2 V(pp), Gain = 2, f = 1 MHz			–69		
V_n	Input voltage noise	f = 10 kHz			2.4		nV/√Hz
I_n	Input current noise	f = 10 kHz	I_{n+}		11		nV/√Hz
			$I_{n–}$		15		
	Differential gain error	Gain = 2, NTSC	R_L = 150 Ω		0.016%		
			R_L = 25 Ω		0.020%		
	Differential phase error	Gain = 2, NTSC	R_L = 150 Ω		0.04°		
			R_L = 25 Ω		0.30°		
	Crosstalk	f = 1 MHz, Gain = 2, R_F = 1.1 kΩ			–62		dB
DC PERFORMANCE							
$Z_{(t)}$	Open loop transimpedance	R_L = 1 kΩ			2		MΩ
V_{IO}	Input offset voltage	T_A = +25°C			1.5	5	mV
		T_A = full range				7	
	Offset voltage drift					10	µV/°C
	Differential offset voltage	T_A = +25°C			0.5	3	mV
		T_A = full range				6	
I_{IB}	Negative input bias current	T_A = +25°C			1.5	9	µA
		T_A = full range				12	
	Positive input bias current	T_A = +25°C			1.5	9	
		T_A = full range				12	
INPUT CHARACTERISTICS							
V_{ICR}	Input common-mode voltage			±13.2	±13.4		V
CMRR	Common-mode rejection ratio	T_A = full range		64	72		dB
r_I	Input resistance	Inverting terminal			15		Ω
		Noninverting terminal			400		kΩ
	Differential input capacitance				1.4		pF

(1) Full power bandwidth = slew rate/2π V_{PEAK}.
(2) Slew rate is defined from the 25% to the 75% output levels.

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ELECTRICAL CHARACTERISTICS (continued)

At $V_{CC(L)}$ = ±5 V, $V_{CC(H)}$ = ±15 V, R_L = 25 Ω, and T_A = +25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS		THS6032 MIN	THS6032 TYP	THS6032 MAX	UNIT
OUTPUT CHARACTERISTICS								
V_O	Output voltage	Single-ended	R_L = 25 Ω		±10.5	±11		V
		Differential	R_L = 50 Ω		±21	±22		
I_O	Output current(3)		R_L = 25 Ω		400	440		mA
I_{SC}	Short-circuit current(3)					800		mA
POWER SUPPLY								
V_{CC}	Supply voltage		$V_{CC(L)}$		0	±5	$\pm V_{CCH}$	V
			$V_{CC(H)}$		±5	±15	±16.5	
I_{CC}	Quiescent current (per amplifier)		$V_{CC(L)}$	T_A = +25°C		4.3	5.8	mA
				T_A = full range			6.2	
			$V_{CC(H)}$	T_A = +25°C		4	5	mA
				T_A = full range			5.5	
PSRR	Power-supply rejection ratio		$V_{CC(L)}$	T_A = +25°C	90	100		dB
				T_A = full range	80			
			$V_{CC(H)}$	T_A = +25°C	69	80		dB
				T_A = full range	66			
SHUTDOWN CHARACTERISTICS								
V_{IL}	Shutdown voltage for power up		Relative to DGND terminal				0.8	V
V_{IH}	Shutdown voltage for power down		Relative to DGND terminal		2			V
I_{IH}	Shutdown input current high		$V_{(SHDN)}$ = 5 V			200	300	µA
I_{IL}	Shutdown input current low		$V_{(SHDN)}$ = 0.5 V			20	40	µA
Z_O	Output impedance (while in shutdown state)		$V_{(SHDN)}$ = 2.5 V, f = 1 MHz			0.5		Ω
I_{CCL}	Supply current (per amplifier) (while in shutdown state)		$V_{(SHDN)}$ = 2.5 V, V_O = 0 V			0.05	0.2	mA
I_{CCH}						2.4	3	
t_{dis}	Disable time(4)					1.1		µs
t_{en}	Enable time(4)					1.5		µs

(3) A heat sink is required to keep junction temperature below absolute maximum when an output is heavily loaded or shorted. See *Absolute Maximum Ratings* table.

(4) Disable/enable time begins when the logic signal is applied to the shutdown terminal and ends when the supply current has reached half of its final value.

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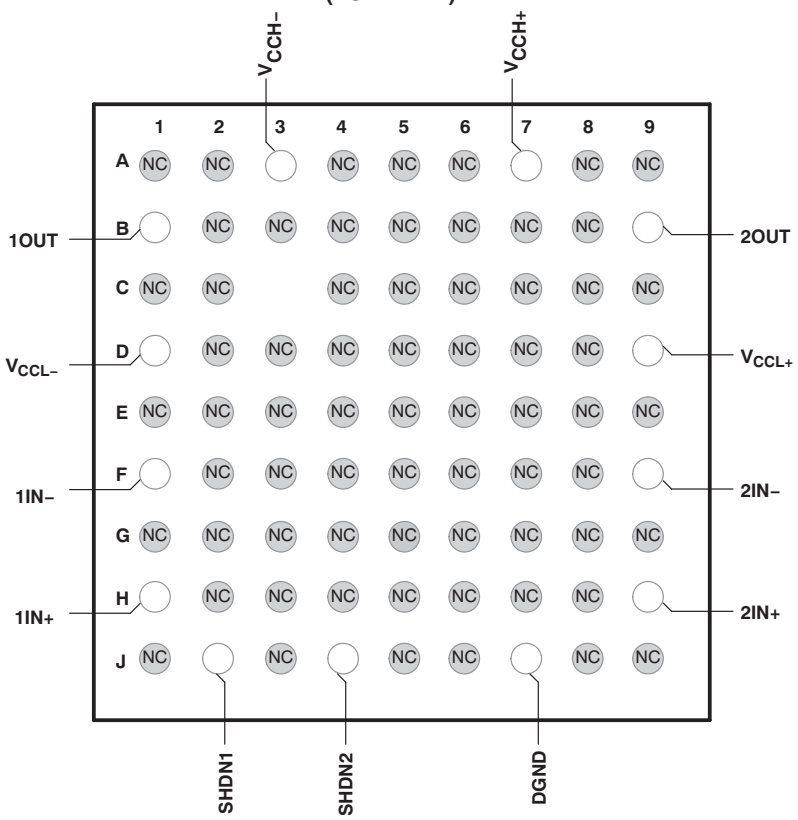
TERMINAL FUNCTIONS

NAME	TERMINAL		
	DWP PACKAGE TERMINAL NO.	GQE PACKAGE TERMINAL NO.	VFP PACKAGE TERMINAL NO.
1OUT	3	B1	1
1IN–	5	F1	5
1IN+	6	H1	7
2OUT	18	B9	24
2IN–	16	G9	20
2IN+	15	H9	18
$V_{CCH–}$	2	A3	30
V_{CCH+}	19	A7	27
$V_{CCL–}$	4	D1	3
V_{CCL+}	17	D9	22
SHDN1	8	J2	10
SHDN2	9	J4	11
DGND	12	J7	14
PAD	1, 10, 11, 20	N/A	N/A
NC	7, 13, 14	N/A	N/A

PIN ASSIGNMENTS

MicroStar Junior (GQE) PACKAGE
(TOP VIEW)



Note: Shaded terminals are used for thermal connection to the ground plane.

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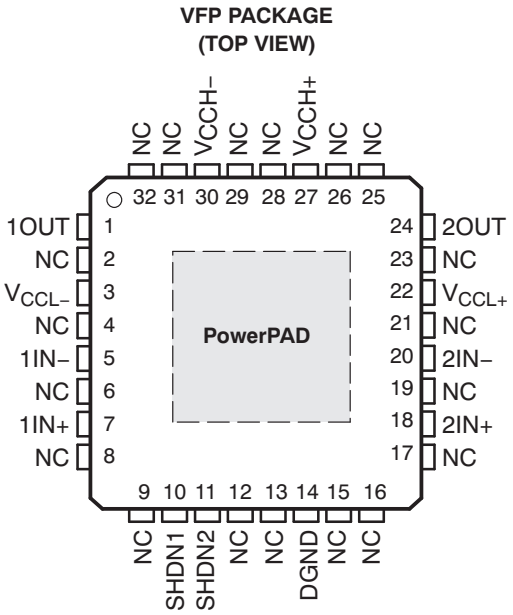
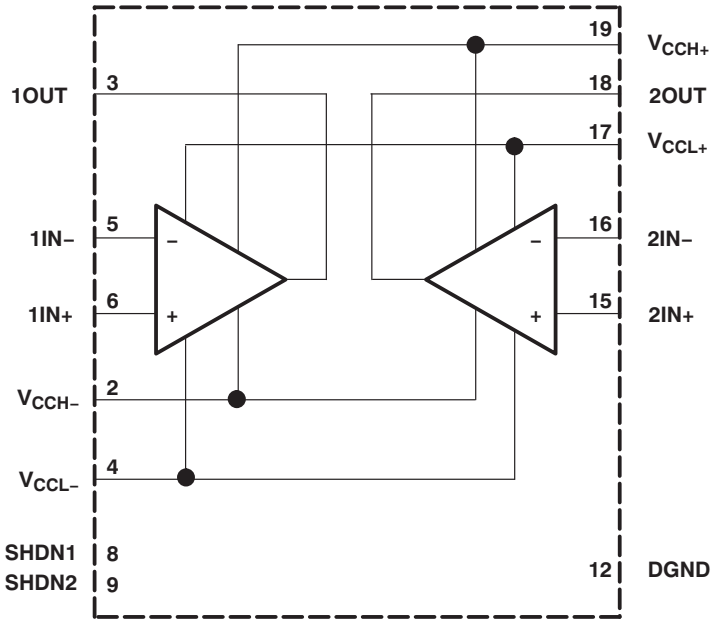


NC – No internal connection

FUNCTIONAL BLOCK DIAGRAM (SOIC PACKAGE)



A. Terminals 1, 10, 11, and 20 are internally connected to the thermal pad.

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

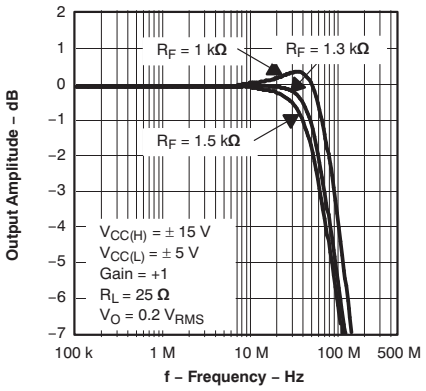


Figure 1.

OUTPUT AMPLITUDE vs FREQUENCY

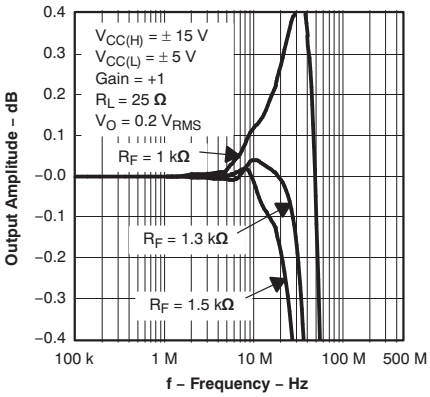


Figure 2.

OUTPUT AMPLITUDE vs FREQUENCY

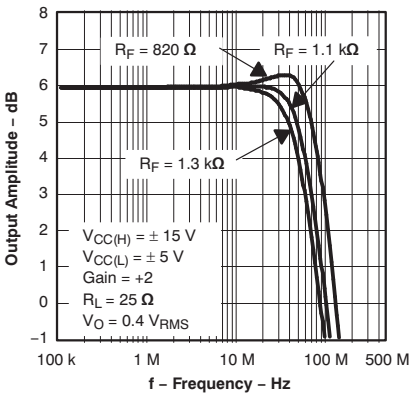


Figure 3.

OUTPUT AMPLITUDE vs FREQUENCY

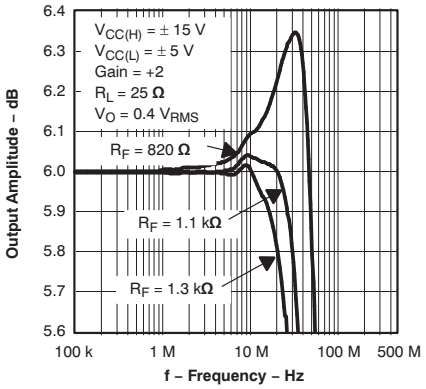


Figure 4.

OUTPUT AMPLITUDE vs FREQUENCY

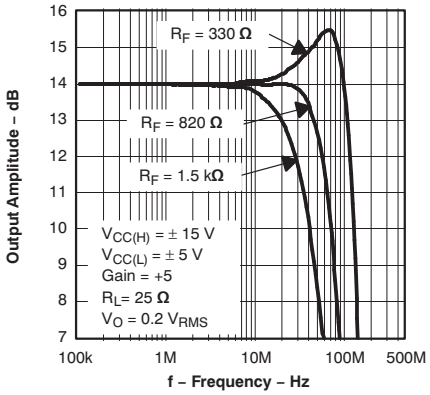


Figure 5.

OUTPUT AMPLITUDE vs FREQUENCY

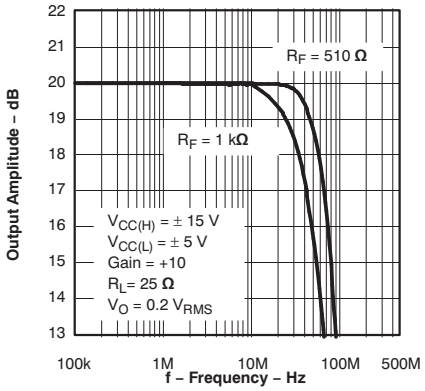


Figure 6.

CLASS-AB MODE OUTPUT AMPLITUDE vs FREQUENCY

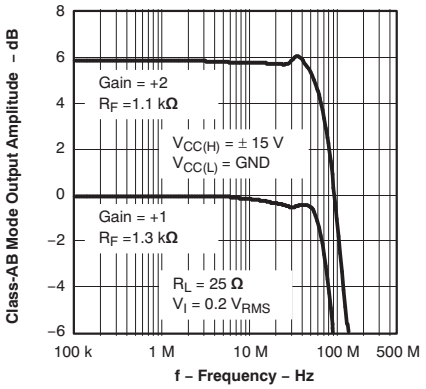


Figure 7.

OUTPUT AMPLITUDE vs FREQUENCY

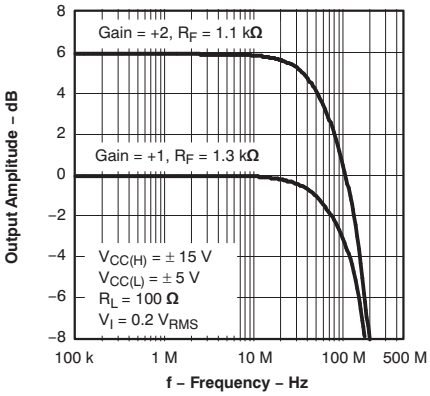


Figure 8.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

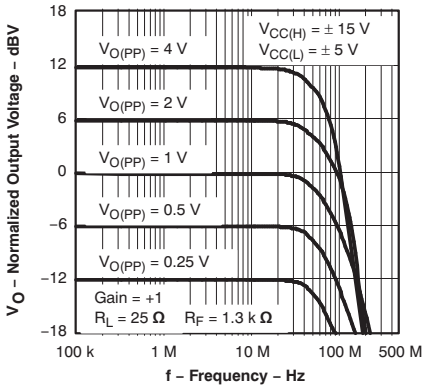


Figure 9.

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TYPICAL CHARACTERISTICS (continued)

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

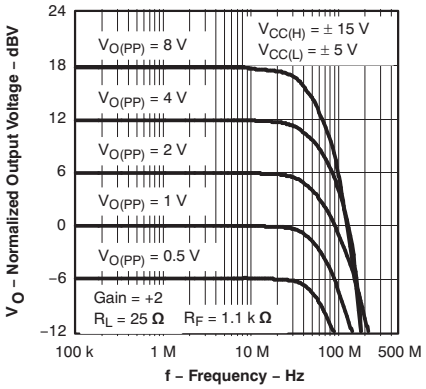

Figure 10.

CLASS-G MODE DISTORTION vs FREQUENCY

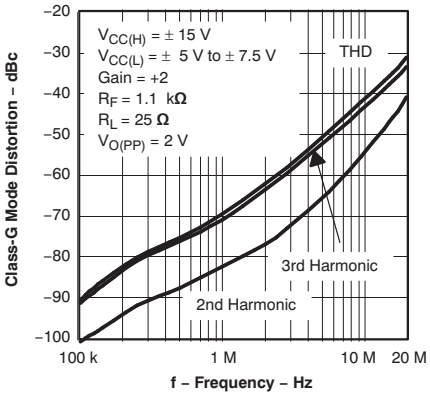

Figure 11.

CLASS-AB MODE DISTORTION vs FREQUENCY

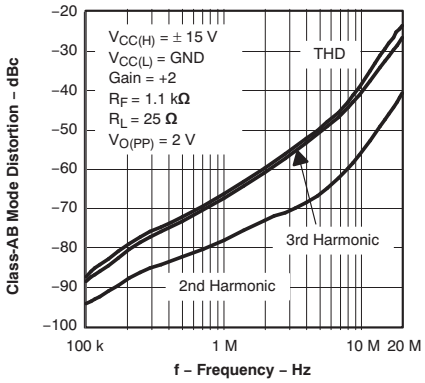

Figure 12.

2ND ORDER DISTORTION vs OUTPUT VOLTAGE

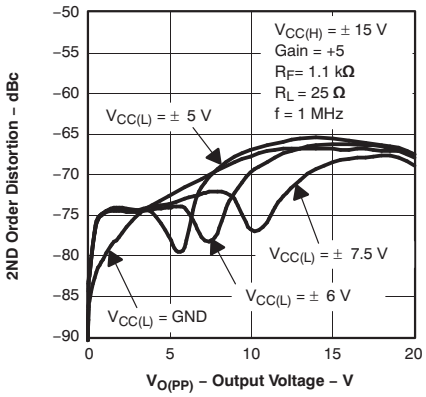

Figure 13.

3RD ORDER DISTORTION vs OUTPUT VOLTAGE

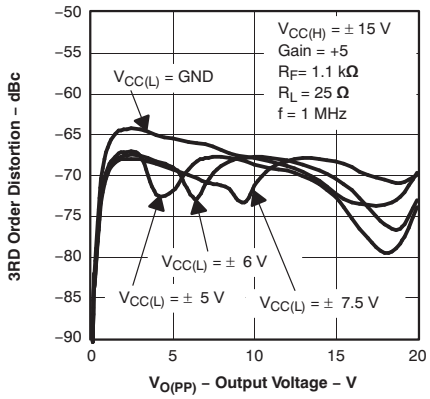

Figure 14.

THD vs OUTPUT VOLTAGE

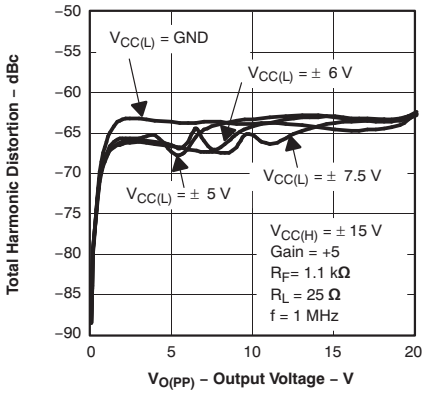

Figure 15.

CROSSTALK vs FREQUENCY

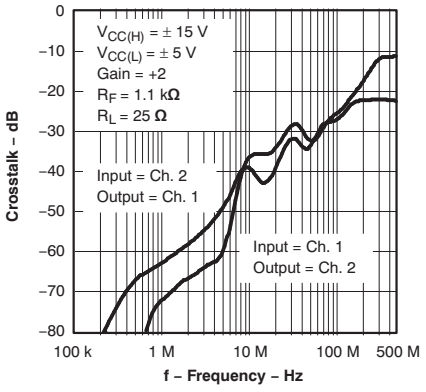

Figure 16.

SLEW RATE vs OUTPUT VOLTAGE STEP

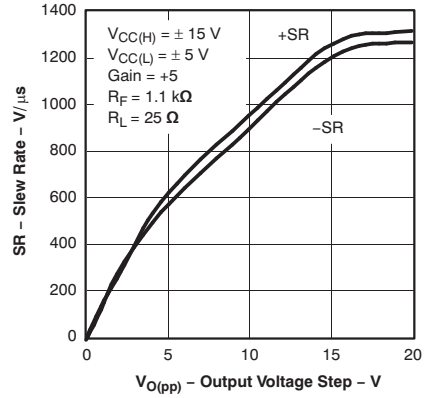

Figure 17.

VOLTAGE AND CURRENT NOISE vs FREQUENCY

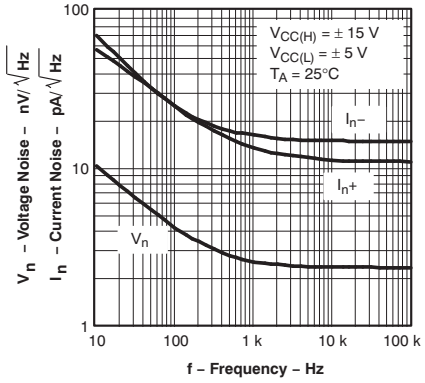

Figure 18.

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TYPICAL CHARACTERISTICS (continued)

TRANSIMPEDANCE vs FREQUENCY

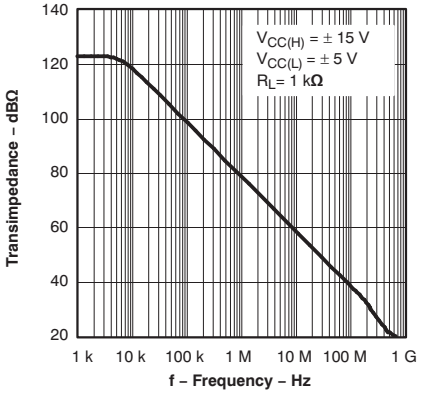

Figure 19.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

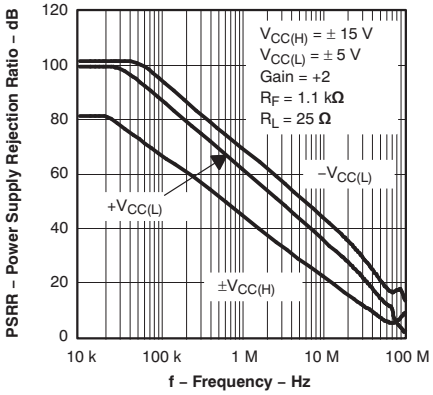

Figure 20.

COMMON-MODE REJECTION RATIO vs FREQUENCY

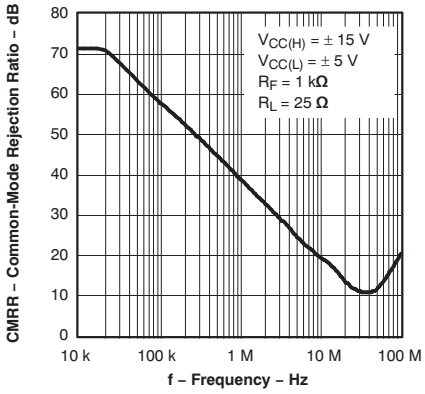

Figure 21.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

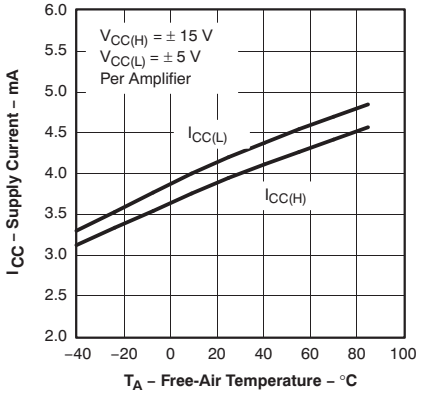

Figure 22.

MAXIMUM OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

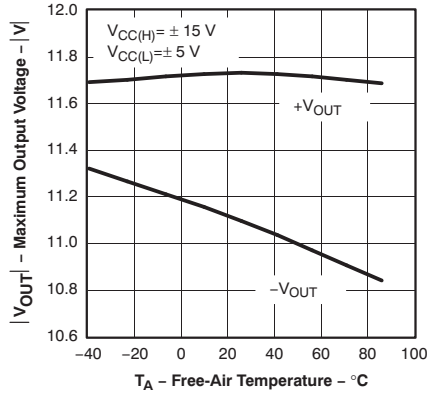

Figure 23.

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

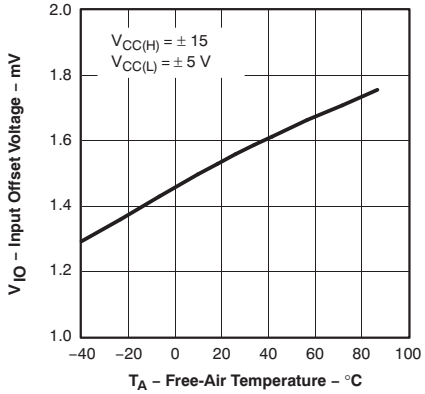

Figure 24.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

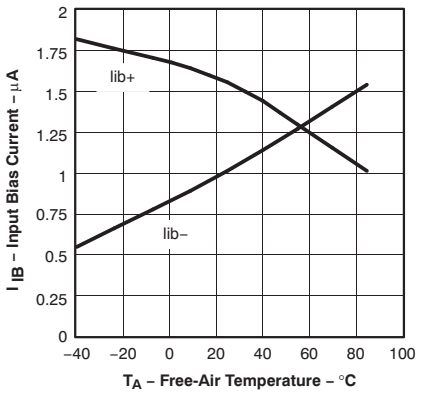

Figure 25.

DIFFERENTIAL GAIN vs LOADING

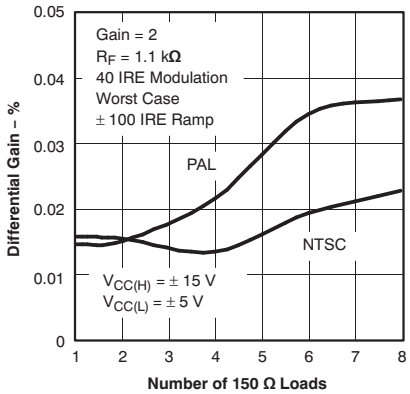

Figure 26.

DIFFERENTIAL PHASE vs LOADING

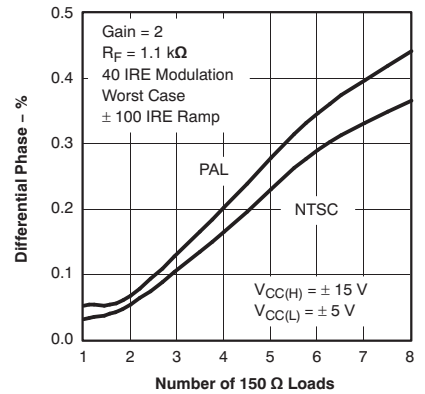

Figure 27.

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TYPICAL CHARACTERISTICS (continued)

CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

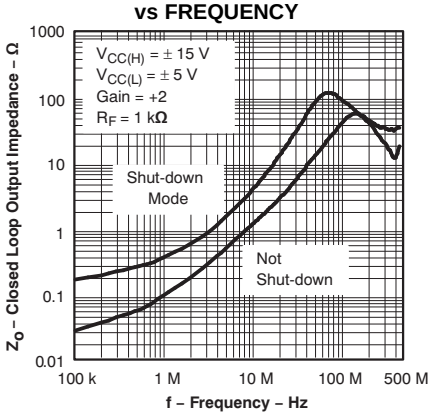

Figure 28.

STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE

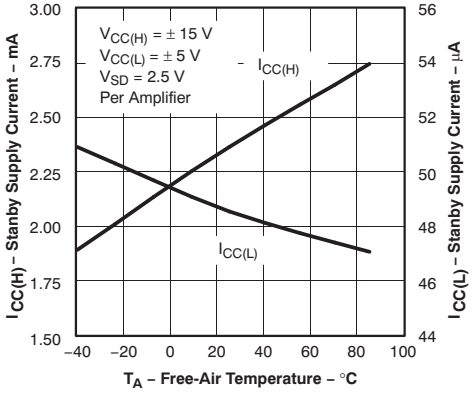

Figure 29.

SHUTDOWN ISOLATION vs FREQUENCY

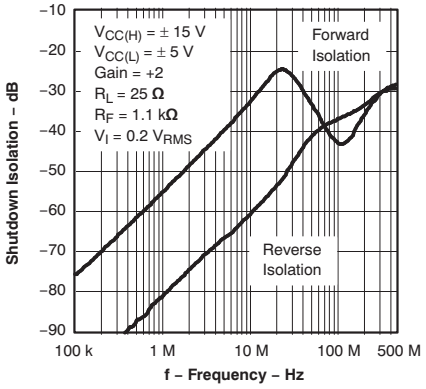

Figure 30.

SHUTDOWN ISOLATION vs FREQUENCY

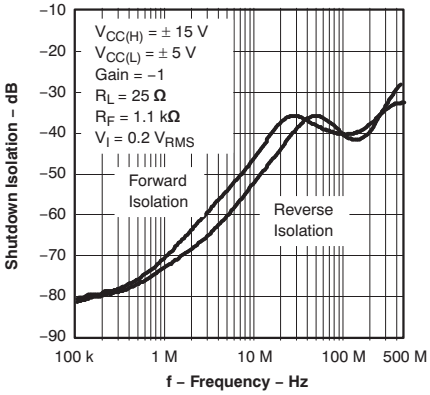

Figure 31.

SHUTDOWN RESPONSE

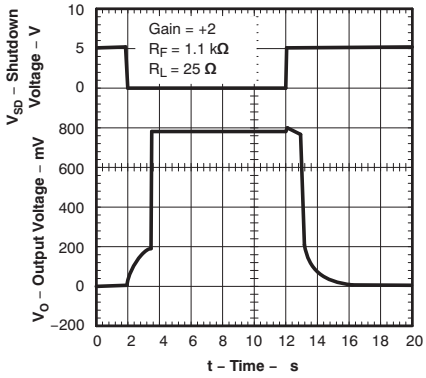

Figure 32.

1-V STEP RESPONSE

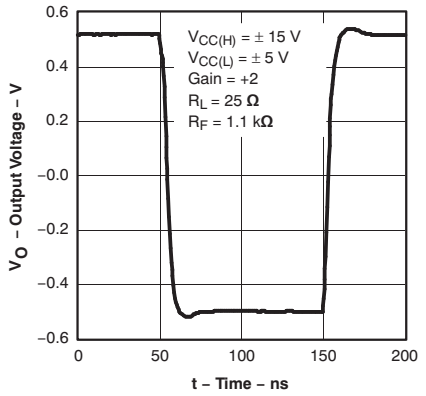

Figure 33.

5-V STEP RESPONSE

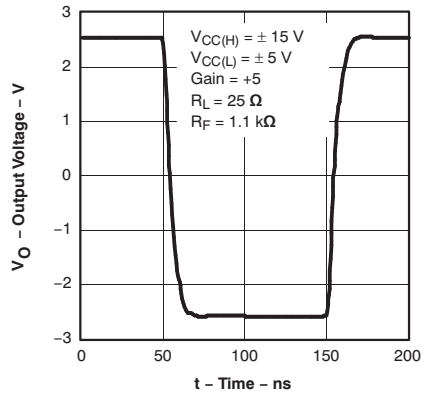

Figure 34.

10-V PULSE RESPONSE

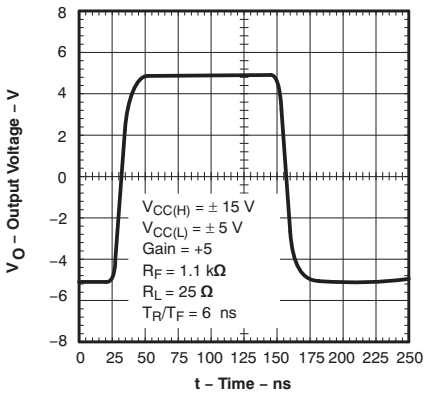

Figure 35.

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APPLICATION INFORMATION

ADSL

The THS6032 was primarily designed as a low-power line driver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 20 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6032 is specified for a minimum full output current of 400 mA at its full output voltage of approximately 11 V. This performance meets the demanding needs of ADSL at the central office end of the telephone line. A typical ADSL schematic is shown in Figure 36.

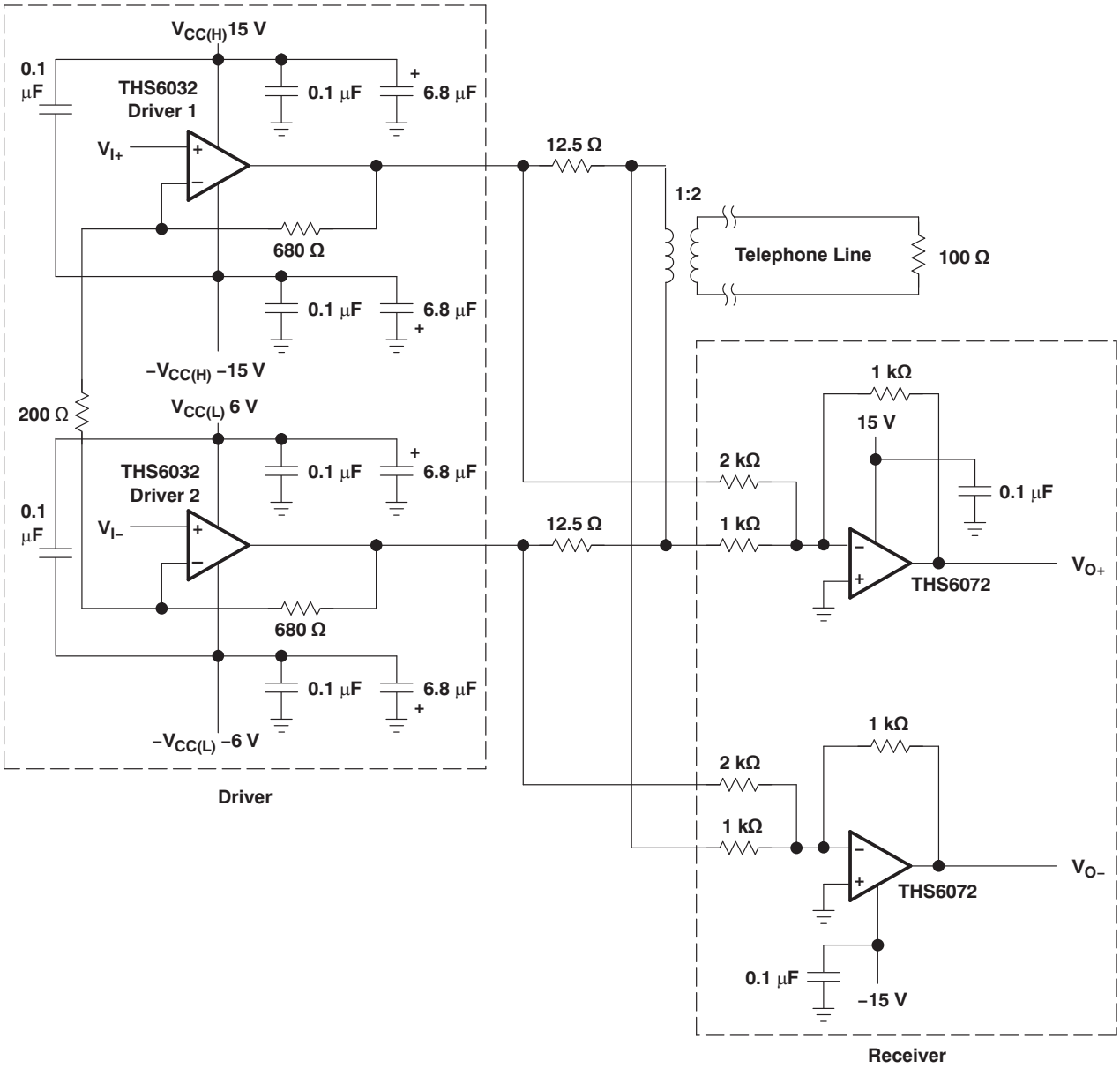

Figure 36. THS6032 ADSL Application

The ADSL transmit band consists of 255 separate carrier frequencies, each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

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The THS6032 has been specifically designed for ultra low distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figure 11 through Figure 15. It is commonly known that in the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. Additionally, distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

One problem that has been receiving a lot of attention in the ADSL area is power dissipation. One way to substantially reduce power dissipation is to lower the power supply voltages. This is because the RMS voltage of an ADSL central office signal is 1.65-V RMS at each driver's output with a 1:2 transformer. But, to meet ADSL requirements, the drivers must have a voltage peak-to-RMS crest factor of 5.6 in order to keep the bit-error probability rate below 10^{-7}. Hence, the power supply voltages must be high enough to accomplish the driver's peak output voltage of 1.65 V × 5.6 = 9.25 $V_{(PEAK)}$.

This high peak output voltage requirement, coupled with a low RMS voltage requirement, does not lend itself to conventional high efficiency designs. One way to save power is to decrease the bias currents internal to the amplifier. The drawback of doing this is an increase in distortion and a lower frequency response bandwidth.

This is where the THS6032 class-G architecture is useful. The class-G output stage utilizes both a high supply voltage [$V_{CC(H)}$ typically ± 15 V] and a low supply voltage [($V_{CC(L)}$ typically ± 6 V]. As long as the output voltage is less than [$V_{CC(L)}$ – 2.5 V], then part of the output current will be drawn from the $V_{CC(L)}$ supplies. If the output signal goes above this cutoff point [for example, $V_O > V_{CC(L)} – 2.5$ V], then all of the output current will be supplied by $V_{CC(H)}$.

To ensure that the cutoff point does not introduce distortion into the system, the entire output stage is always biased on. This constant biasing scheme will cause a decrease in the efficiency over hard switching class-G circuits, but the very low distortion results tend to outweigh the efficiency loss. The biasing scheme used in the THS6032 can be shown by the currents being supplied by the $V_{CC(L)}$ power supplies in Figure 37. This graph shows there is no discrete current transfer point between the $V_{CC(L)}$ supplies and the $V_{CC(H)}$ supplies. This was done to ensure low distortion throughout the entire output range. By changing the $V_{CC(L)}$ supply voltage, the system efficiency can be tailored to suit almost any system with high crest factor requirements.

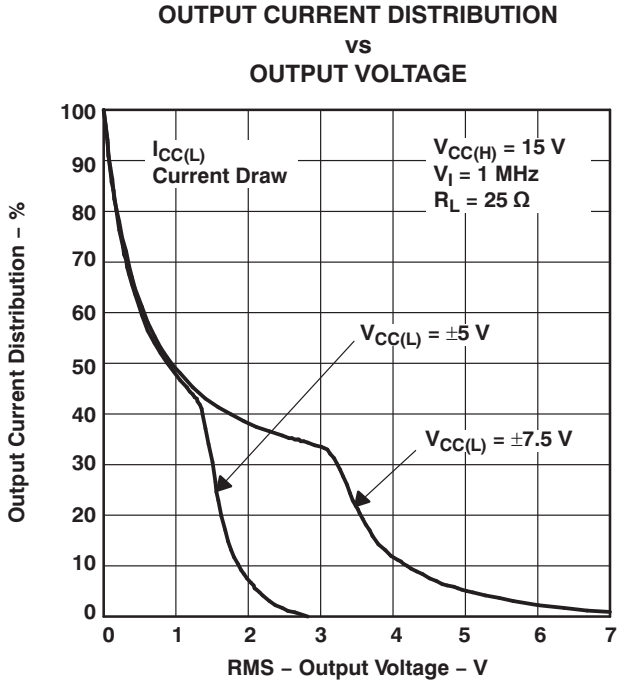


Figure 37.

CLASS-AB MODE OPERATION

The class-G architecture produces sizable power dissipation savings over traditional class-AB designs while maintaining low distortion requirements. The only drawback to the class-G design is the requirement of 4 power supply voltages, 2 more than a typical line driver requires. In certain instances, the addition of two separate power supplies may be cost prohibitive or PCB space prohibitive. In these cases there are two options, use a traditional amplifier, such as a THS6012, or use the THS6032 in class-AB mode.

Using the THS6032 in class-AB mode will give several functional benefits over the THS6012. This includes shutdown capability, low-impedance output while in shutdown state, and a slight reduction in quiescent current. One important thing to remember is that the THS6032 running in class-AB mode, will be only about as efficient as the THS6012. This means that the power dissipation of the THS6032 will increase dramatically and must be accounted for. Failure to do so will result in a part which continuously overheats and may lead to failure.

To use the THS6032 in class-AB mode, the user should always connect the $V_{CC(L)}$ power supply pins to GND. The internal $V_{CC(L)}$ paths were not designed for continuous full output current and could possibly fail. The $V_{CC(H)}$ paths were designed for the full output currents and thus, should be used for class-AB mode operation.

The performance of the THS6032 while in class-AB mode is very similar to the class-G mode. Figure 7 and Figure 12 show THS6032 performance while in class-AB mode.

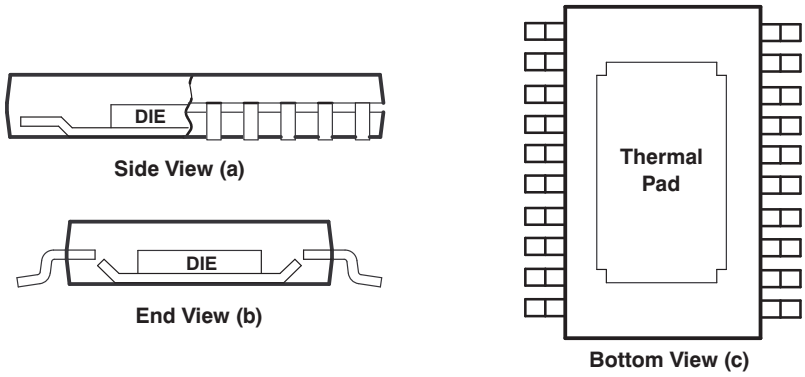
DEVICE PROTECTION FEATURES

The THS6032 has two built-in features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the high supply rails [$\pm V_{CC(H)}$] can cause failure of the device and is not recommended.

The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately +180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the junction temperature drops below +150°C, the internal thermal shutdown circuit automatically turns the device back on.

THERMAL INFORMATION

The THS6032 is available in a thermally-enhanced DWP package and a VFP package, which are members of the PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 38(a) and Figure 38(b) for the DWP views]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 38©)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 38. Views of Thermally-Enhanced DWP Package

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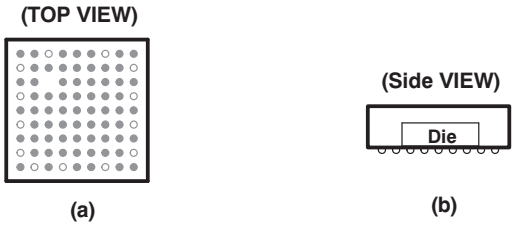
The THS6032 is also available in the MicroStar Junior GQE package. Just like the DWP and VFP packages, the GQE package utilizes the PowerPAD functionality to improve thermal performance. The GQE package is part of the new ball-grid array (BGA) family developed by Texas Instruments (TI). This package allows for even higher-density layouts with virtually no loss in thermal performance. Its construction is similar to the DWP and VFP construction [see Figure 39 (a) and (b)], but uses the terminal balls to transfer the heat away from the die.



NOTE: Shaded areas are part of the thermally-conductive path.

Figure 39. Views of Thermally-Enhanced GQE Package

The PowerPAD packages allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads or balls are being soldered), the thermal areas can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the PCB design considerations section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heat sinking.

Because of its power dissipation, proper thermal management of the THS6032 is required. There are several ways to properly heat sink all three PowerPAD packages. There are several TI application notes on how to best accomplish the thermal mounting scheme required for each package. For the DWP and VFP packages, refer to the Texas Instruments Technical Brief, *PowerPAD Thermally-Enhanced Package* (SLMA002). There is also a more compact technical paper entitled *PowerPad Made Easy* (SLMA004). For the GQE – MicroStar Junior package, refer to the *MicroStar BGA Packaging Reference Guide* (SSYZ015A) and the compact version entitled *MicroStar Junior Made Easy* (SSYA009). This literature is available on TI's web site at http://www.ti.com.

The actual thermal performance achieved with the THS6032 in its PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 21.5°C/W for the DWP package, 37.8°C/W for the GQE package, and 30°C/W for the VFP package. Although the maximum recommended junction temperature (T_J) is listed as +150°C, performance at this elevated temperature will suffer. To ensure optimal performance, the junction temperature should be kept below +125°C. Above this temperature, distortion will tend to increase. Figure 40 shows the recommended power dissipation with a junction temperature of +125°C. Also shown is what happens if no solder is used to solder the PowerPAD to the PCB. The θ_{JA} increases dramatically with a vast reduction in power dissipation. For a given θ_{JA} and a maximum junction temperature, the power dissipation is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (1)$$

Where:

P_D = Power dissipation of THS6032 (watts)

T_{MAX} = Maximum junction temperature allowed in the design (+125°C recommended)

T_A = Free-ambient air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case (DWP = 0.37°C/W, GQE = 4.56°C/W, VFP = 1.2°C/W)

θ_{CA} = Thermal coefficient from case to ambient

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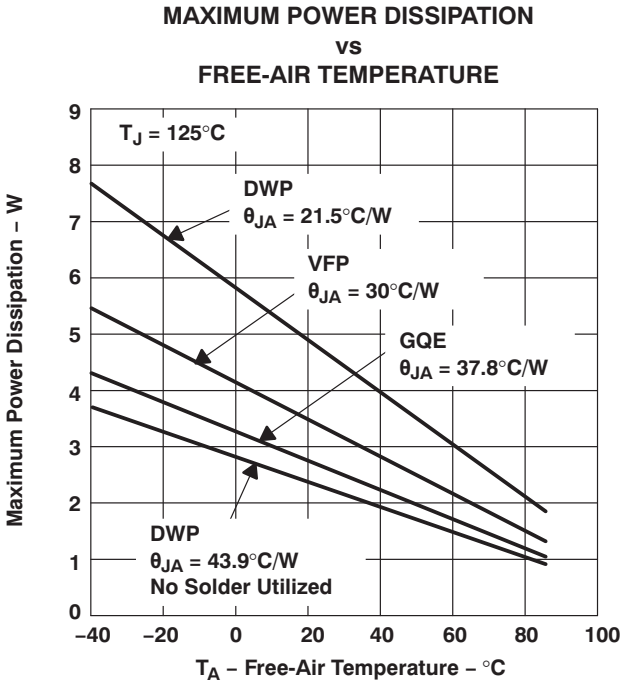

Figure 40. Maximum Power Dissipation vs Free-Air Temperature

PCB DESIGN CONSIDERATIONS

Proper PCB design techniques in two areas are important to assure proper operation of the THS6032. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6032 is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low-inductance ground connection. Although a ground connection directly to a terminal of the THS6032 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low-inductance ground to the device substrate to minimize internal crosstalk, and it provides a path for heat removal.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 41, which shows what happens when a 2.2 pF capacitor is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. While the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a virtual ground and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 42, where a 27-pF capacitor adds only 2.5 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initially appear to be a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. Therefore, proper analysis of adding a capacitor to the inverting input node should always be performed to ensure stable operation.

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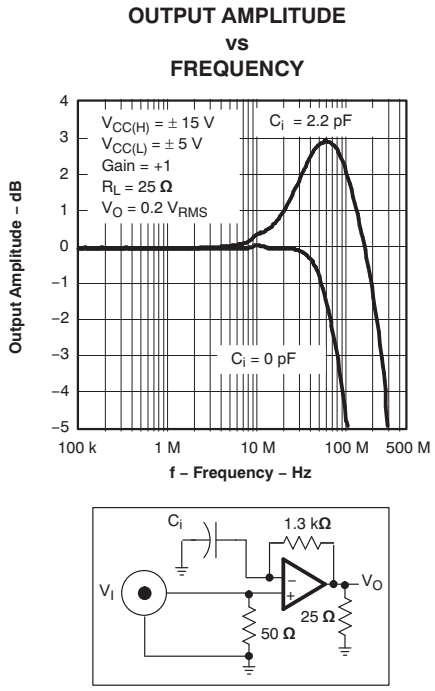

Figure 41.

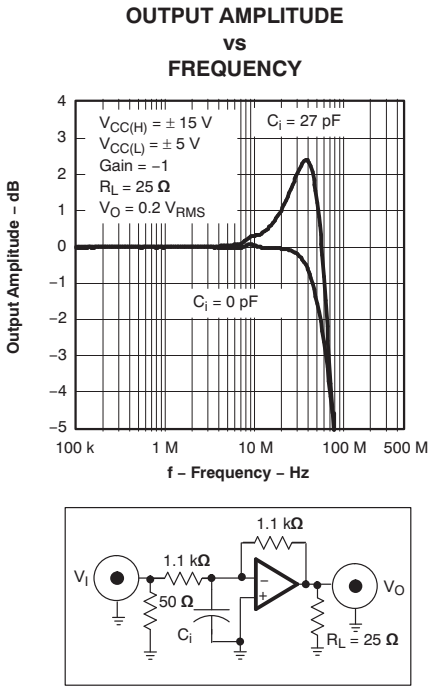

Figure 42.

- Proper power supply decoupling – Use a minimum of a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum capacitor among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.
- Differential power supply decoupling – The THS6032 was designed to drive low-impedance differential signals. The 25-Ω load that each amplifier drives causes large amounts of current to flow from amplifier to amplifier. Power-supply decoupling for differential-currents must be provided to ensure low distortion in the THS6032. By simply connecting a 0.1-µF ceramic capacitor from the $+V_{CC(H)}$ pin to the $–V_{CC(H)}$ pin, along with another 0.1-µF ceramic capacitor from the $+V_{CC(L)}$ pin to the $–V_{CC(L)}$ pin, differential current loops will be minimized (see Figure 36). This will help keep the THS6032 operating at peak performance.

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current feedback amplifiers, the bandwidth of the THS6032 is an inversely-proportional function of the value of the feedback resistor. This can be seen from Figure 1 to Figure 6. The recommended resistors for the optimum frequency response with a 25-Ω load system can be seen in Table 1. These should be used as a starting point. When optimum values are found, 1%- tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback-resistor value of 1.3 kΩ is recommended; this value provides a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Consistent with current-feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and the internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current-feedback amplifiers over conventional voltage-feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third-order harmonic distortion increases more than the second-order harmonic distortion.

Table 1. Recommended Feedback Resistor Values for 25-Ω Loads

GAIN	R_f
1	1.3 kΩ
2, –1	1.1 kΩ
5	820 kΩ
7.8	680 kΩ
10	510 kΩ

SHUTDOWN CONTROL

There are two shutdown pins that control the shutdown for each amplifier of the THS6032. When the shutdown pin signals are low, the THS6032 is active. But, when a shutdown pin is high (≥2 V), the corresponding amplifier is turned off. The shutdown logic is not latched, and should always have a signal applied to it. To help ensure a fixed logic state, an internal 50-kΩ resistor to DGND is utilized. An external resistor, such as a 3.3 kΩ, to DGND may be added to help improve noise immunity in harsh environments. If no external resistor is used and $SHDN_X$ pins are left unconnected, the THS6032 defaults to a power-on state. A simplified circuit is shown in Figure 43.

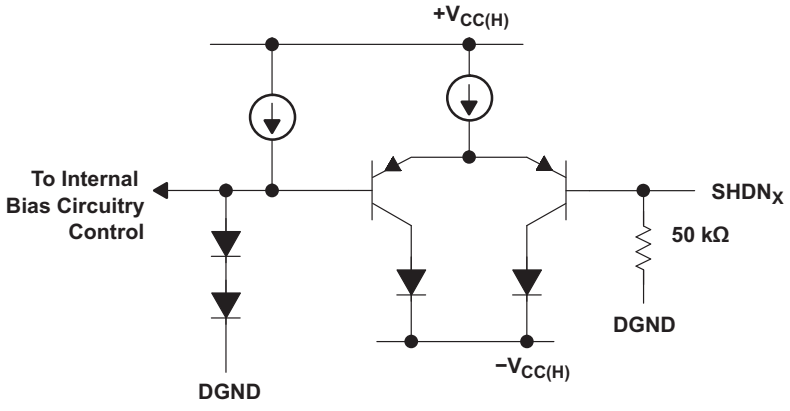

Figure 43. Simplified THS6032 Shutdown Control Circuit

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SHUTDOWN FUNCTION

The THS6032 incorporates a shutdown circuit to conserve power. Traditionally, when an amplifier is placed into shutdown mode, the input and output circuitry are turned off. This conserves a large amount of power, but the output impedance will be a very high, typically greater than several kΩ. This situation does not maintain proper line termination, resulting in a severe reduction of the receive signal coming through the transmission line (see Figure 36).

The THS6032 eliminates this problem. When the $SHDN_X$ pin voltage is greater than 2 V, the THS6032 enters shutdown mode to conserve power. Unlike the traditional amplifier, the THS6032's output impedance is typically 0.5 Ω at 1 MHz (see Figure 28). The shutdown mode function results in the proper termination of the line with no degradation in performance of the receive signal coming through the transmission line.

There are a few design considerations that must be observed in order to fully achieve this type of functionality. To better understand these design considerations, it is helpful to examine what is happening inside the THS6032. Figure 44 shows the simplified shutdown components. Notice that there are two similar input stages; the normal input stage consisting of transistors Q1 through Q4 and the shutdown input stage consisting of transistors QS1 through QS4. When in shutdown mode, the $I_{(BIAS - 1)}$ and $I_{(BIAS - 2)}$ current sources are turned off. This turns off the normal input stage of the amplifier. The $I_{(BIAS - S1)}$ and $I_{(BIAS - S2)}$ current sources are then turned on. The shutdown input stage signals are then fed through the same internal circuitry which the normal input stage drove. This allows for sinking and sourcing large amounts of current at the output of the THS6032 during shutdown operation. The QS1 through QS4 transistors are not designed for performance like the Q1 through Q4 transistors, because their only function is to amplify the DC ground reference, DGND. A 1-kΩ resistor connects internally to the output node of the amplifier, which provides a feedback loop in shutdown mode. This forces the output impedance to become very small, allowing proper transmission line termination.

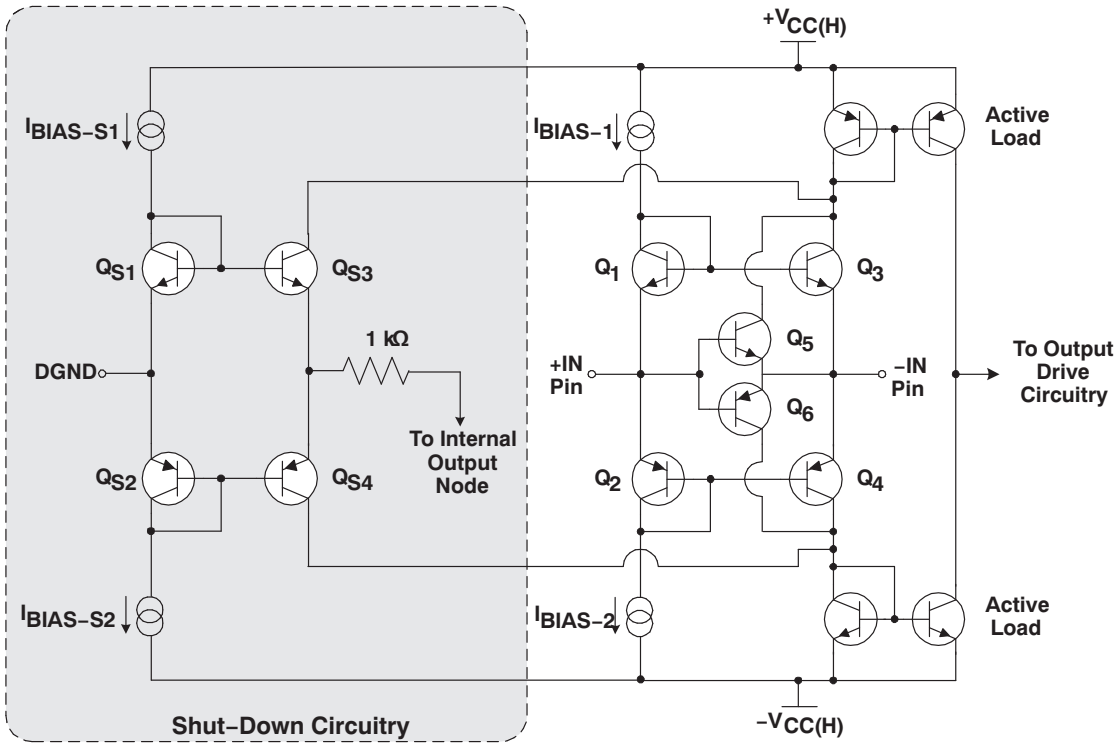

Figure 44. Simplified THS6032 Input Stages

Because the DGND-pin voltage is effectively a noninverting terminal, any signal or voltage fluctuation at this node is amplified by the THS6032. This could possibly cause a noisy output to appear during shutdown operation. Figure 45 shows the frequency response of the THS6032 due to an input signal at the DGND terminal. The maximum DGND voltage signal which the THS6032 will follow linearly during shutdown operation is less than ±4 V. With this dynamic range capability, it is recommended that the DGND pin be as noise-free as possible to ensure proper transmission line termination.

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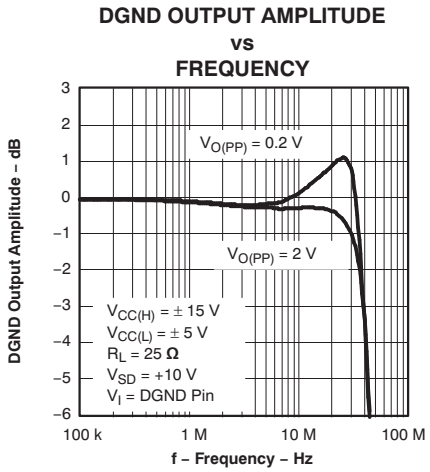

Figure 45.

The second design consideration is due to transistors Q_5 and Q_6. These transistors ensure that the +IN to –IN voltage separation is less than a V_{BE} drop (about 0.7 V). This protects the other transistors, Q_1 to Q_4, from saturating during fast transients. Transistors Q_5 and Q_6 also enhance the slew rate capabilities of the THS6032. When a fast transient is applied to the input, these transistors quickly apply the currents to the active load stages. A design issue with this setup is that while in shutdown mode, a large enough signal being applied to the input pins may turn on these transistors. Once the input voltage differential between the +IN and –IN pins reaches ±0.7-V, transistors Q_5 and Q_6 turn on, applying the difference signal to the rest of the amplifier circuitry. Because these two transistors are designed for much higher performance levels than the shutdown circuitry transistors (Q_{S3} and Q_{S4}), they will become dominant and the difference input signal will be utilized instead of the DGND signal. Because the external negative feedback resistor path is still connected around the amplifier, this difference input signal will be amplified just like a normal amplifier is designed to do (see Figure 46). As long as the +IN and –IN input signals are kept below ±0.7 V, the isolation from input-to-output is very high, as shown in the Shutdown Isolation vs Frequency graphs (see Figure 30 and Figure 31).

To ensure proper shutdown functionality of the THS6032, it is important to keep the DGND voltage noise-free. Additionally, the +IN and –IN signals should be limited to less than ±0.7 V during shutdown mode. This will ensure proper line termination functionality while conserving power.

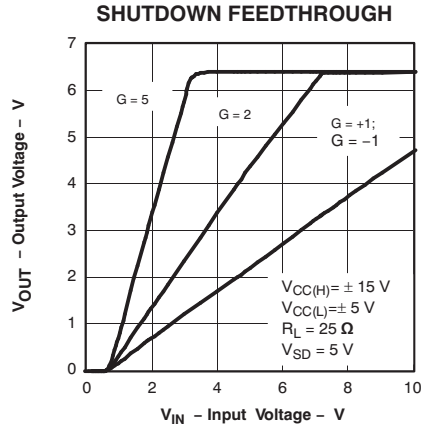

Figure 46.

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SLEW RATE

The slew rate performance of a current-feedback amplifier like the THS6032 is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors should help the PCB designer arrive at a more optimum circuit with fewer problems.

Whether the THS6032 is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. Slew rate performance in the inverting configuration is generally faster than the noninverting configuration. This is because in the inverting configuration the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes further degrades the slew rate, simply because there is more capacitance to charge. If the main supply voltage $V_{CC(H)}$ to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes. Also, as the load resistance decreases, the slew rate typically decreases due to the increasing internal currents, which slow down the transitions.

Internally, the THS6032 has other factors that impact the slew rate. The amplifier's behavior during the slew rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1200 V/µs are processed by the input stage in a very linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. For slew rates greater than 1200 V/µs, additional slew-enhancing transistors present in the input stage (transistors Q5 and Q6 in Figure 44) begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew rate capabilities. The additional aberrations present in the output waveform with these faster slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20 ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input signal slew rate reduces the effect.

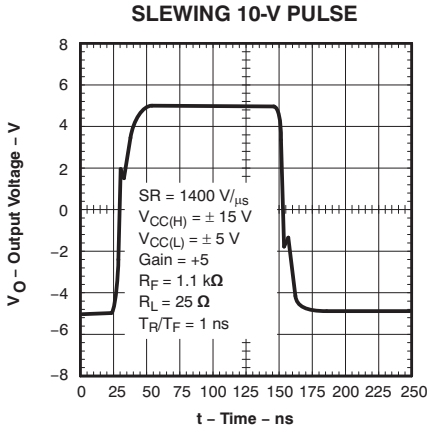

Figure 47.

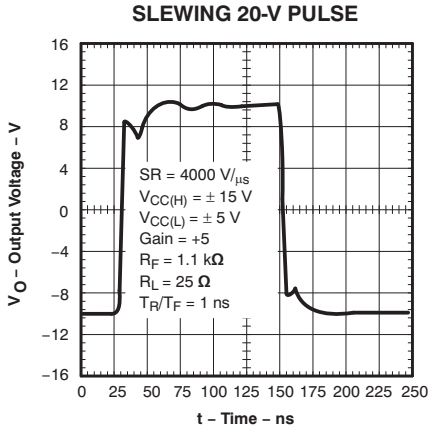

Figure 48.

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NOISE CALCULATIONS AND NOISE FIGURE

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input, while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 49. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/√Hz)
- IN+ = Noninverting current noise (pA/√Hz)
- IN– = Inverting current noise (pA/√Hz)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

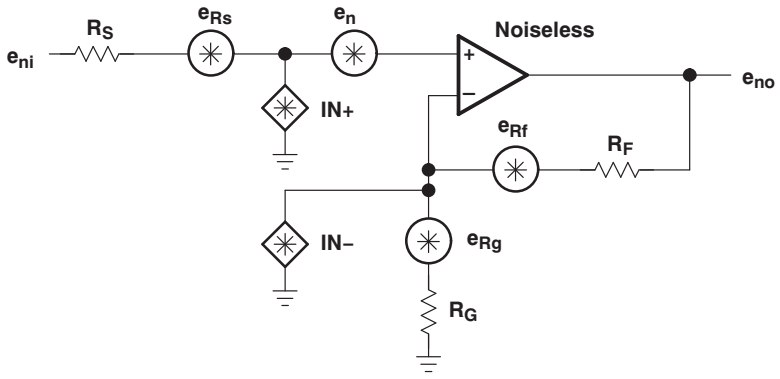

Figure 49. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)} \quad (2)$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)} \quad (3)$$

As the previous equations show, to keep noise at a minimum, small-value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal-amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier.

For more information on noise analysis, refer to *Noise Analysis in Operational Amplifier Circuits* (SLVA043A).

Another noise measurement usually preferred in RF applications is the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined, and is typically 50 Ω in RF applications.

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$$NF = 10\log\left[\frac{e_{ni}^{2}}{(e_{Rs})^{2}}\right] \quad (4)$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[(e_n)^2 + (IN + \times R_S)^2\right]}{4\,kTR_S}\right] \quad (5)$$

Figure 50 shows the noise figure graph for the THS6032.

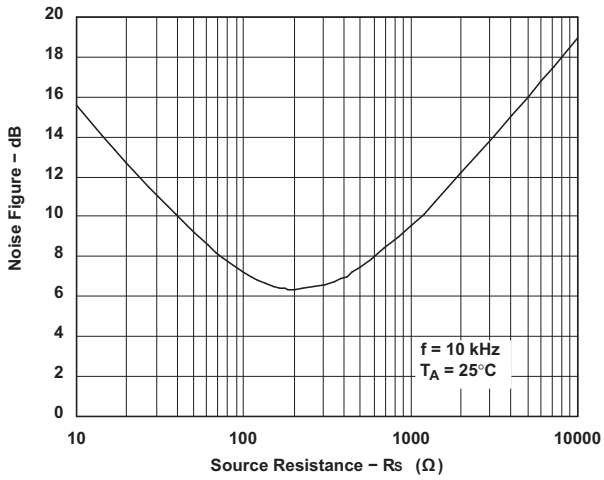
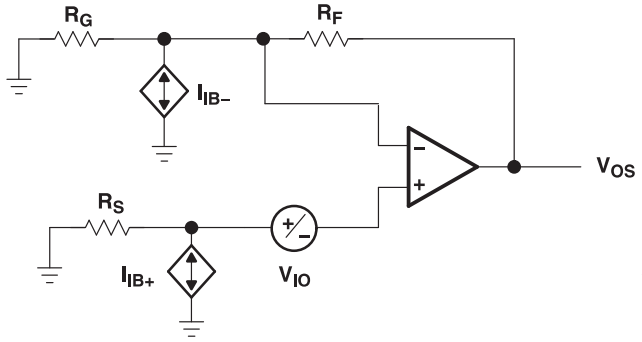


Figure 50. Noise Figure vs Source Resistance

OFFSET VOLTAGE

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input-bias currents (I_{IB}) times the corresponding gains. Figure 51 can be used to calculate the output offset voltage.



$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 51. Output Offset Voltage Model

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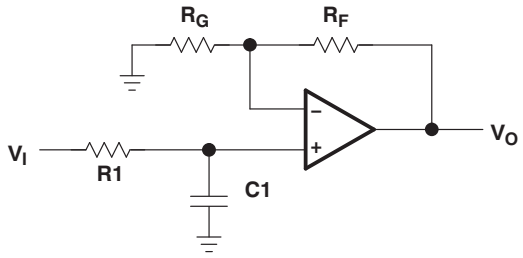
GENERAL CONFIGURATIONS

A common error for the first-time CFB user is to create a unity-gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates, so this is not recommended. The THS6032, like all CFB amplifiers, must have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier, and should not be considered when using a current-feedback amplifier. Because of this, simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 52).

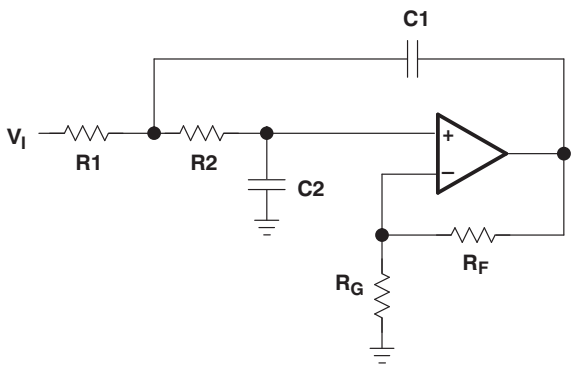


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left[\frac{1}{(1 + sR1C1)}\right]$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 52. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. One implementation of the Sallen-Key filter is shown in Figure 53. For more information on Sallen-Key filters, refer to the *Analysis of the Sallen-Key Architecture* (SLOA024A).



R1 = R1 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 53. 2-Pole Low-Pass Sallen-Key Filter

Another good use for the THS6032 amplifier is as a video distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

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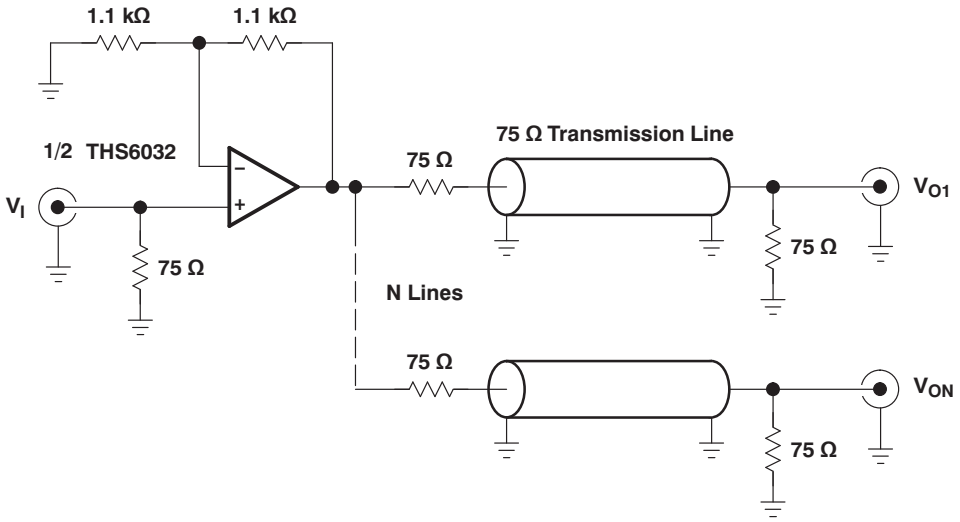

Figure 54. Video Distribution Amplifier Application

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6032 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 55. A minimum value of 10 Ω should work well for most applications. For example, in ADSL systems, setting the series resistor value to 12.5 Ω both isolates any capacitance loading and provides the proper line-impedance matching at the source end.

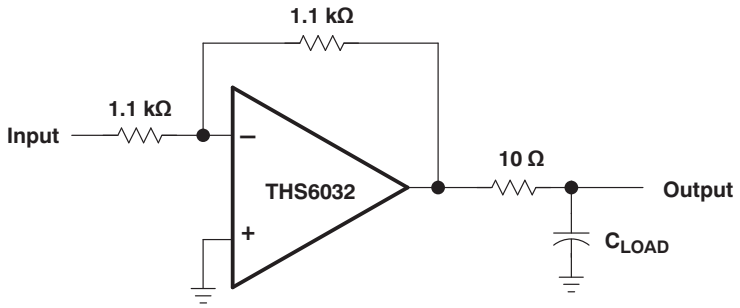

Figure 55. Driving a Capacitive Load

EVALUATION BOARD

Evaluation boards are available for the THS6032. Each board has been configured for proper thermal management of the THS6032 depending on package selection. The circuitry has been designed for a typical ADSL application as shown previously in this document. To order the evaluation board, contact your local TI sales office or distributor.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October, 2007) to Revision F **Page**

- Removed *Product Preview* sidebar stamp; device and document are at production data status 1
- Corrected typical value for *Differential phase error* (typo) 4

Changes from Revision D (May, 2001) to Revision E **Page**

- Updated document format to current standards 1
- Changed Figure 51 to correct errors in circuit design 23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6032CDWP	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS6032C	Samples
THS6032IDWP	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6032I	Samples
THS6032IDWPR	ACTIVE	SO PowerPAD	DWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6032I	Samples
THS6032IGQER	OBSOLETE	BGA MICROSTAR JUNIOR	GQE	80		TBD	Call TI	Call TI	-40 to 85		
THS6032IVFPG4	ACTIVE	HLQFP	VFP	32		TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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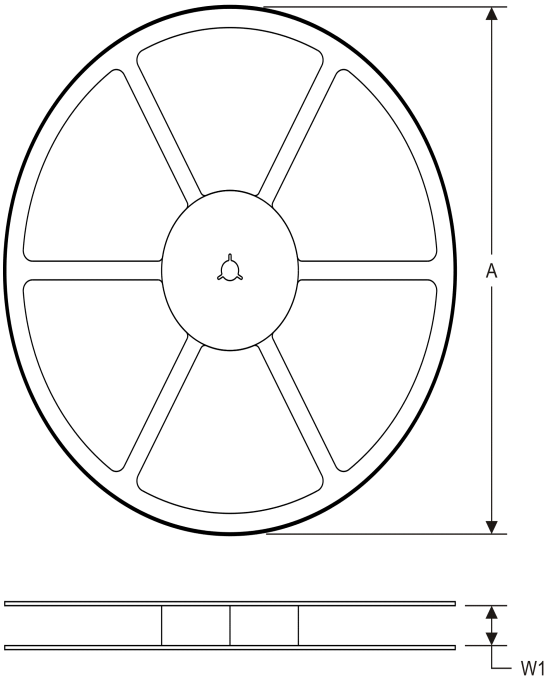
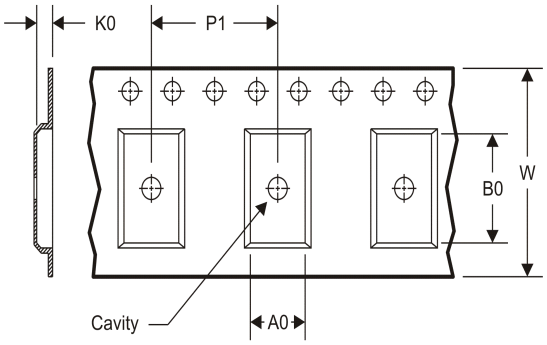
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



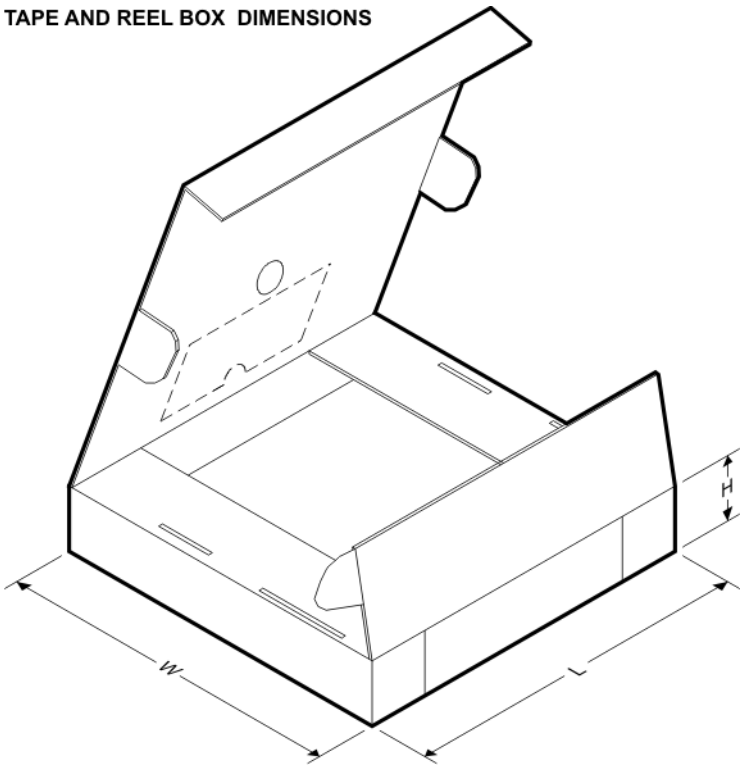
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6032IDWPR	SO Power PAD	DWP	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

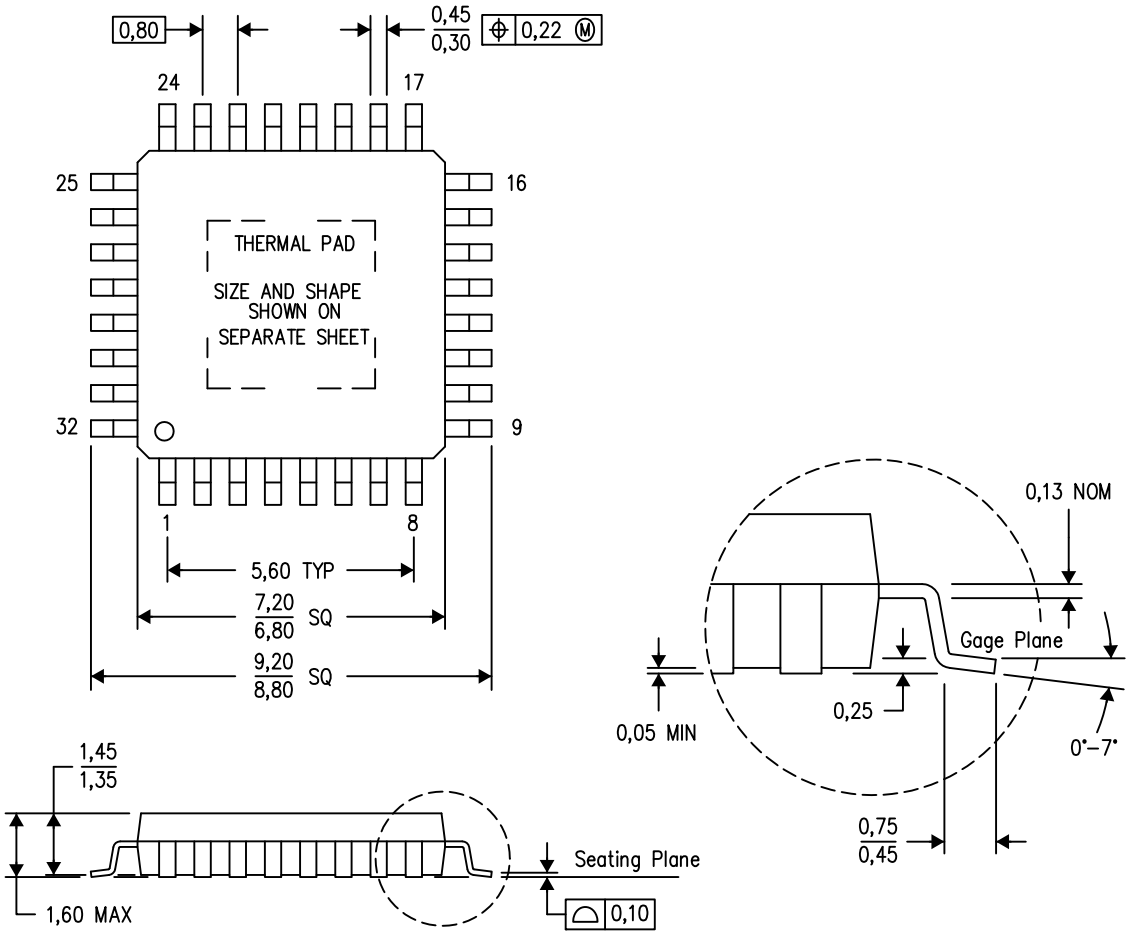
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6032IDWPR	SO PowerPAD	DWP	20	2000	367.0	367.0	45.0

VFP (S–PQFP–G32) PowerPAD™ PLASTIC QUAD FLATPACK

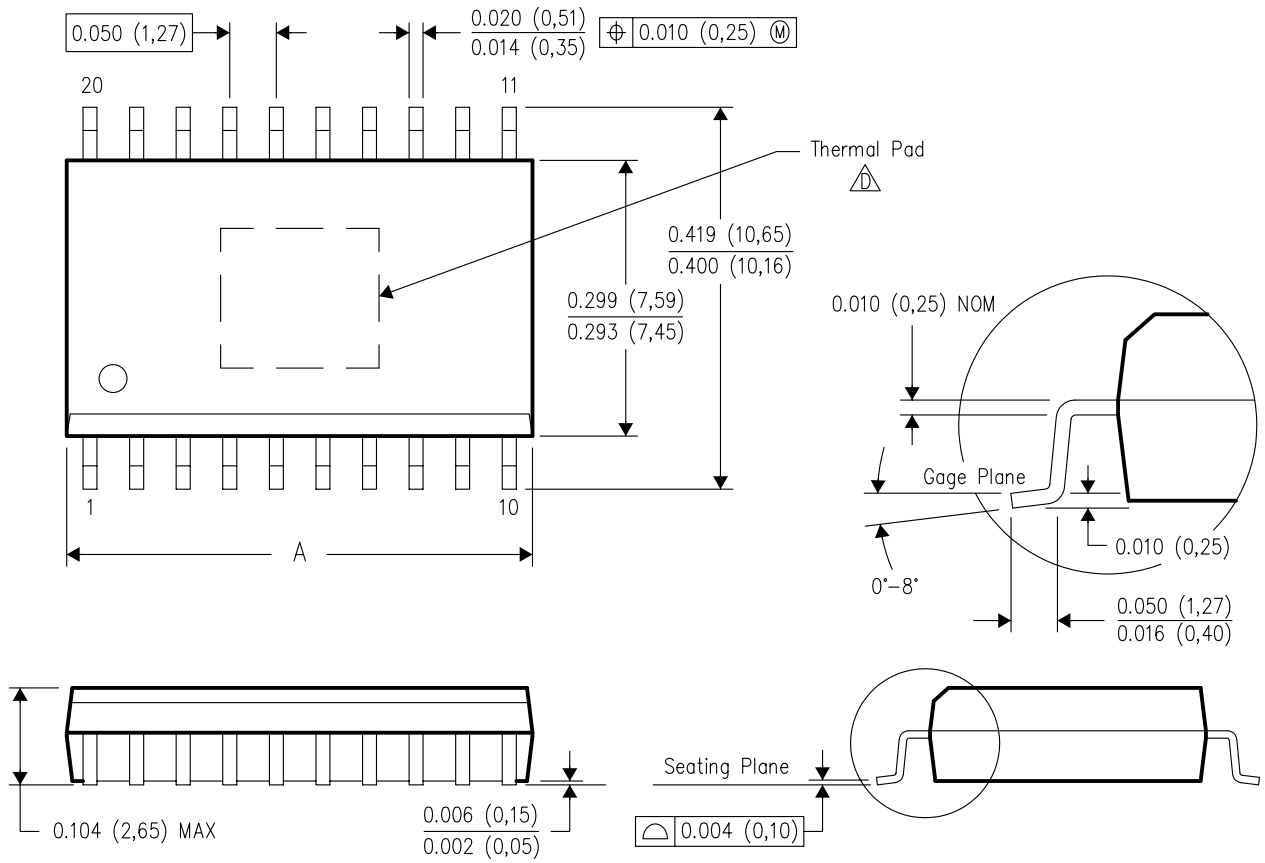


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments Incorporated.

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

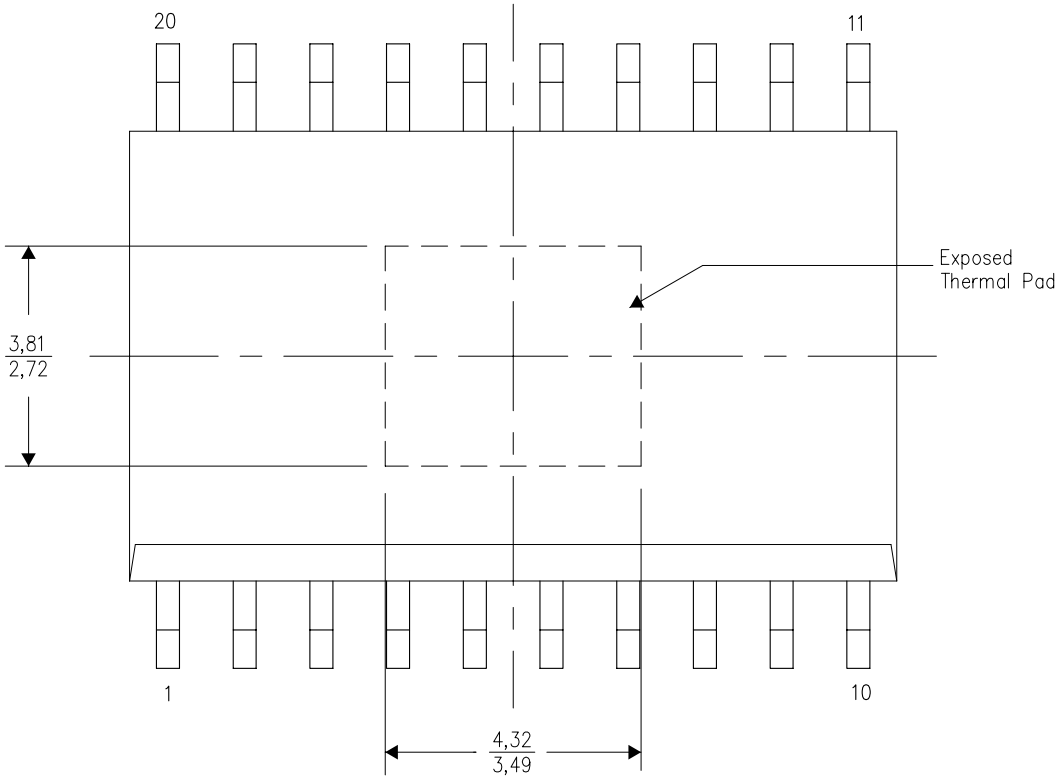
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206325–2/E 12/10

NOTE: A. All linear dimensions are in millimeters

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